[0069] Furthermore, the difference **126***a* can be controlled by a combination of the width pf each column and the impurity concentration of each column.

[0070] Although the semiconductor device is a MOSFET (i.e., metal oxide silicon field effect transistor), the semiconductor device can be another device such as an IGBT (i.e., insulated gate bipolar transistor), a SIT (i.e., static induction transistor) and a SBT (i.e., shottky barrier diode).

[0071] Although the N column **25**, **25***a*, **25***b* and the P column **27**, **27***a*, **27***b* have a rectangular shape, the N and the P columns can have other shape such as a thin plate shape, a quadrangular prism shape, and a hexagonal cylinder shape. Further, although the N columns **25**, **25***a*, **25***b* and the P columns **27**, **27***a*, **27***b* are alternately aligned, the second columns can be dispersed in the first region instead of the first column, the first region which spreads in the plane perpendicular to the thickness direction. Thus, the device includes at least the first region and the second region, a pair of which is repeated alternately in one direction.

[0072] Here, U.S. Pat. No. 6,844,592 discloses that the difference of the impurity amount of the N column and the P column in the periphery region is homogeneous. Accordingly, the device shown in **FIG. 1** having the difference of the impurity amount of the N column and the P column, which is distributed in the periphery region, is different from U.S. Pat. No. 6,844,952. The distribution of the difference is such that the difference of the impurity amount in the inner periphery region is different, i.e., larger than that in the outer periphery region.

[0073] Specifically, in the device disclosed in U.S. Pat. No. 6,844,952, when the impurity amount of the first region and the second region is deviated, the withstand voltage of the device is rapidly reduced. However, in the present invention, even when the impurity amount of the first region and the second region is deviated, the withstand voltage of the device is not rapidly reduced.

[0074] Further, in the present invention, the inner periphery region and the outer periphery region are disposed to surround the centre region in this order, so that the depletion layer homogeneously expands from the center region to the periphery region. Furthermore, the inner periphery region is disposed to protrude from the source electrode, so that the depletion is performed in the periphery region completely.

[0075] While the invention has been described with reference to preferred embodiments thereof, it is to be understood that the invention is not limited to the preferred embodiments and constructions. The invention is intended to cover various modification and equivalent arrangements. In addition, while the various combinations and configurations, which are preferred, other combinations and configurations, including more, less or only a single element, are also within the spirit and scope of the invention.

What is claimed is:

1. A semiconductor device comprising:

a center region, in which a semiconductor switching device is disposed;

a periphery region surrounding the center region; and

a semiconductor layer including a plurality of pairs of a first region having a first conductive type and a second region having a second conductive type, wherein

the semiconductor layer is disposed from the center region to the periphery region,

the first and the second regions extend in a thickness direction of the device,

the first and the second regions are alternately aligned in a plane perpendicular to the thickness direction of the device,

the first region includes a first impurity amount, and the second region includes a second impurity amount,

the periphery region includes an utmost outer periphery pair of the first and the second regions and an utmost inner periphery pair of the first and the second regions,

the utmost inner periphery pair is disposed next to the center region, and the utmost outer periphery pair is disposed on outmost of the periphery region,

the utmost outer periphery pair has a difference between the second impurity amount of the second region and the first impurity amount of the first region, the difference which is smaller than a maximum difference between the second impurity amount and the first impurity amount of another pair of the first and the second regions in the periphery region, and

the utmost inner periphery pair has a difference between the second impurity amount of the second region and the first impurity amount of the first region, the difference which is larger than a difference between the second impurity amount and the first impurity amount of a pair of the first and the second regions in the center region.

2. The device according to claim 1, wherein

the difference between the second impurity amount and the first impurity amount of a pair in the periphery region becomes larger as it goes from the utmost outer periphery pair to the utmost inner periphery pair, and

the difference between the second impurity amount and the first impurity amount of a pair in the center region is smaller than the difference between the second impurity amount and the first impurity amount of the utmost inner periphery pair.

3. The device according to claim 1, wherein

the first region in each of the center and the periphery regions has a constant width in a repeat direction of the first and the second regions,

the second region in each of the center and the periphery regions has a constant width in the repeat direction of the first and the second regions, and

the difference between the second impurity amount and the first impurity amount is controlled by at least one of the impurity concentrations of the first region and the second region.

4. The device according to claim 1, wherein

the utmost outer periphery pair of the first and the second regions in the periphery region has a sum of the first and the second impurity amounts of the first region and the second region, and